subtraction. In addition, the receiver must run before the transmitter in order to maintain the maximum latency at two buffer times. An event triggered at the time of the first sample of a buffer received during a time slice K−1, will be detected during processing in slice K. The answer may appear as the first sample of the buffer transmitted during slice K+1. Thus, if the transmitter had run before the receiver, then the event might only have been responded to in the first sample of the buffer transmitted in slice K+2, making the latency three buffer times.

Therefore, echo canceler processing on delayed transmitter data is performed first (step **70**). Then receiver processing is performed on the difference between the received samples from time slice K−1 and the samples generated by the echo canceler process in slice K (step **72**). Finally, transmit processing is performed, generating a buffer full of samples to be transmitted during time slice K+1 (step **74**) and stored in delay registers **35**.

Thus, utilizing the buffer switching mechanism of the present invention, resistance to interrupt latency can be maximized. In the example provided above, buffers of size **256** at 8000 samples/sec yields 32 ms buffer times. Assuming thirty percent processing period gives a maximum interrupt latency of 22.4 ms, which provides a very large time margin. In addition, a side benefit of using long buffers is lowered CPU utilization in terms of lowered overhead enabling the CPU to perform other functions. The main benefit provided by the present: invention is the ability of an NSP modem to conform to the strict time constraints of the higher bit rate modem standards (e.g., V.32 9600 bps) V.32bis 14,400 bps and V.34 28,800 bps).

In addition, if for any reason one of the modems requests a retrain process during a connection, the buffer size can be changed back to a short buffer size so that a retain process can occur At a later time, the buffer size Is switched back to a larger buffer size.

While the invention has been described with respect to a limited number of embodiments, it will be appreciated that many variations, modifications and other applications of the invention may be made.

What is claimed is:

Please cancel claims 1 – 12.

1. A method, in a communications system, of achieving a balance between processing response time, on one hand, and robustness to interrupt latency and processor implementation overhead, on the other hand, said method comprising of the steps of:

utilizing sample buffers having a first buffer size when it is desired to optimize said communication system so as to have quick processing response times;

utilizing sample buffers having a second buffer size when it is desired to optimize said communication system so as to be robust to interrupt latency and to have low processor implementation overhead; and

providing switching means enabling said communication system to dynamically switch between using said buffers having a first buffer size and said buffers having a second buffer size.

2. The method according to claim 1, wherein the size of said sample buffers is coherently switched without any loss of data.

3. The method according to claim 1, wherein said second buffer size is greater than said first buffer size.

4. The method according to claim 1, wherein the size of said sample buffer is switched to said first buffer size when the modem connection is reinitialized or restarted.

5. The method according to claim 1, wherein the size of said sample buffer is switched to said first buffer size when

a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32 bis and V.34.

6. A system, in a communications system, for achieving a balance between processing response time, on one hand, and robustness to interrupt latency and processor implementation overhead, on the other hand, said system comprising:

means for utilizing sample buffers having a first buffer size when it is desired to optimize said communication system so as to have quick processing response times;

means for utilizing sample buffers having a second buffer size when it is desired to optimize said communication system so as to be robust to interrupt latency and to have low processor implementation overhead; and

switching means enabling said communication system to dynamically switch between using said buffers having a first buffer size and said buffers having a second buffer size.

7. The system according to claim 6, wherein the size of said sample buffers is coherently switched without any loss of data.

8. The system according to claim 1, wherein said second buffer size is greater than said first buffer size.

9. The system according to claim 6, wherein the size of said sample buffer is switched to said first buffer size when the modem connection is reinitialized or restarted.

10. The system according to claim 6, wherein the size of said sample buffer is switched to said first buffer size when a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32 bis and V.34.

11. A method, in a communications system, of achieving a balance between processing response time, on one hand, and robustness to interrupt latency and processor implementation overhead, on the other hand, said communication

system including a receiver. transmitter and associated receive sample buffer and transmit sample buffer. wherein sample processing is divided into time slices within said communication system. said method comprising of the steps of:

utilizing receive and transmit sample buffers having a first buffer size L1 when it is desired to optimize said communication system so as to have quick processing response times;

utilizing receive and transmit sample buffers having a second buffer size L2 when it is desired to optimize said communication system so as to be robust to interrupt latency and to have low processor implementation overhead;

providing switching means enabling said communication system to dynamically switch between using said transmit and receive sample buffers having a size L1 and a size L2;

making a determination to switch buffer sizes before the activation of said transmitter during time slice N;

processing a receive buffer of length L1 and a transmit buffer of length L1 during time slice N−1;

processing a receive buffer of length L1 and a transmit buffer of length L2 during time slice N;

processing a receive buffer of length L1 and a transmit buffer of length L2 during time slice N+1; and

processing a receive buffer of length L2 and a transmit buffer of length L2 during time slice N+2 and during time slices thereafter until such decision to switch buffer sizes.

12. The method according to claim 11. wherein the size of said transmit and receive sample buffers is coherently switched without any loss of data.]

* * * * *

Please add new claims 13-52:

13. A method achieving a balance between response time system latency, said communication system including a receiver, transmitter and associated receive sample buffer and transmit sample buffer, wherein sample processing is divided into time slices within said communication system, said method comprising of the steps of:

employing receive and transmit sample buffers having a first buffer size L1 capable of quick response times;

employing receive and transmit sample buffers having a second buffer size L2 capable of accommodating system latency;

employing a switching device enabling said communication system to dynamically switch between using said transmit and receive sample buffers having a size L1 and a size L2;

making a determination to switch buffer sizes before the activation of said transmitter during time slice N;

processing a receive buffer of length L1 and a transmit buffer of length L1 during time slice N-1;

processing a receive buffer of length L1 and a transmit buffer of length L2 during time slice N;

processing a receive buffer of length L1 and a transmit buffer of length L2 during time slice N+1; and

processing a receive buffer of length L2 and a transmit buffer of length L2 during time slice N+2 and during time slices thereafter until such decision to switch buffer sizes.

14. The method of claim 13, wherein the size of said transmit and receive sample buffers is coherently switched without any loss of data.

15. A system for achieving a balance between response time and system latency in a communication system, said system comprising:

sample buffers having a first buffer size capable of quick response times;

sample buffers having a second buffer size capable of accommodating system latency; and

a switching device capable of dynamically switching between the use of said buffers having a first buffer size and said buffers having a second buffer size.

16. The system of claim 15, wherein said second buffer size is robust so as to accommodate system latency.

17. The system of claim 15, wherein said sample buffers are maintained in a memory.

18. The system of claim 15, wherein said sample buffers are maintained in physical buffers.

19. The system of claim 15, wherein said dynamic switching is performed in response to communication system operating requirements.

20. The system of claim 15, wherein said system latency comprises interrupt latency.

21. The system of claim 15, wherein said system latency comprises bus latency.

22. The system of claim 15, wherein said system latency comprises both interrupt latency and bus latency.

23. The system of claim 15, wherein the size of said sample buffers is coherently switched without any loss of data.

24. The system of claim 15, wherein said second buffer size is greater than said first buffer size.

25. The system of claim 15, wherein the size of said sample buffer is switched to said first buffer size when a modem connection is reinitialized or restarted.

26. The system of claim 15, wherein the size of said sample buffer is switched to said first buffer size when a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32 bis and V.34.

27. A system for achieving a balance between response time and system latency in a communication system, said system comprising of the steps of:

sample buffers having a first buffer size capable of quick response times;

sample buffers having a second buffer size that is robust so as to accommodate system latency; and

a switching device capable of dynamically switching between the use of said buffers having a first buffer size and said buffers having a second buffer size.

28. A system for achieving a balance between response time and system latency in a communication system, said system comprising:

a sample buffer that is variable in size, wherein the sample buffer has a first buffer size capable of quick response times and a second buffer size capable of accommodating system latency; and

a switching device capable of dynamically switching between said first buffer size and said second buffer size of the sample buffer.

29. A machine readable medium containing executable instructions which, when executed by a machine, causes the machine to perform the steps of a method for achieving a balance between response time and system latency in a communication system, the method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size capable of accommodating system latency; and

dynamically switching between the use of

said buffers having a first buffer size and said buffers having a second buffer size.

30. The medium of claim 29, wherein said second buffer size is robust so as to accommodate system latency.

31. The medium of claim 29, wherein said dynamic switching is performed in response to communication system operating requirements.

32. The medium of claim 29, wherein said system latency comprises interrupt latency.

33. The medium of claim 29, wherein said system latency comprises bus latency.

34. The medium of claim 29, wherein said system latency comprises both interrupt latency and bus latency.

35. The medium of claim 29, wherein the size of said sample buffers is coherently switched without any loss of data.

36. The medium of claim 29, wherein said second buffer size is greater than said first buffer size.

37. The medium of claim 29, wherein the size of said sample buffer is switched to said first buffer size when a modem connection is reinitialized or restarted.

38. The medium of claim 29, wherein the size of said sample

buffer is switched to said first buffer size when a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32 bis and V.34.

39. A machine readable medium containing executable instructions which, when executed by a machine, causes the machine to perform the steps of a method for achieving a balance between response time and system latency in a communication system, the method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size that is robust so as to accommodate system latency in said communication system; and

employing a switching device capable of dynamically switching between the use of said buffers having a first buffer size and said buffers having a second buffer size.

40. A machine readable medium containing executable instructions which, when executed by a machine, causes the machine to perform the steps of a method for achieving a balance between response

time and system latency in a communication system, the method comprising:

employing a sample buffer that is variable in size, wherein said sample buffer has a first buffer size capable of quick response times and a second buffer size capable of accommodating system latency; and

employing a switching device capable of dynamically switching between said first buffer size and said second buffer size of said sample buffer.

41. A method of achieving a balance between response time and system latency in a communication system, said method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size capable of accommodating system latency; and

employing a switching device capable of dynamically switching between said buffers having a first buffer size and

said buffers having a second buffer size.

42. The method of claim 41, wherein said second buffer size is robust so as to accommodate system latency.

43. The method of claim 41, wherein said dynamic switching is performed in response to communication system operating requirements.

44. The method of claim 41, wherein said system latency comprises interrupt latency.

45. The method of claim 41. wherein said system latency comprises bus latency.

46. The method of claim 41, wherein said system latency comprises both interrupt latency and bus latency.

47. The method of claim 41, wherein the size of said sample buffers is coherently switched without any loss of data.

48. The method of claim 41, wherein said second buffer size is greater than said first buffer size.

49. The method of claim 41, wherein the size of said sample buffer is switched to said first buffer size when a modem connection is reinitialized or restarted.

50. The method of claim 41, wherein the size of said sample buffer is switched to said first buffer size when a retrain sequence has

been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32 bis and V.34.

51. A method of achieving a balance between response time and system latency in a communication system, said method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size that is robust so as to accommodate system latency in said communication system; and

employing a switching device capable of dynamically switching between said buffers having a first buffer size and said buffers having a second buffer size.

52. A method of achieving a balance between response time and system latency in a communication system, said method comprising:

employing a sample buffer that is variable in size, wherein said sample buffer has a first buffer size capable of quick response times and a second buffer

size capable of accommodating system latency; and

employing a switching device capable of dynamically switching between said buffers having a first buffer size and said buffers having a second buffer size.